UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BRIAN R. MEARS, MARK N. FULLERTON, and
NICHOLAS J. KOHOUT

Appeal 2007-0399
Application 09/961,024[1]
Technology Center 2100

Decided: June 25, 2007

Before KENNETH W. HAIRSTON, LANCE LEONARD BARRY, and JAY P. LUCAS, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

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[1] Application filed 09/21/01. Application PCT/US02/29075 is a continuation of this application. The real party in interest is the Intel Corporation.

Appellants appeal from a Final Rejection of claims 1 to 14, 16 to 18, 28 to 31, 33 to 44, and 49 under authority of 35 U.S.C. § 134. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a method and circuit for a multiple channel communications bus interface to minimize the number of inter-chip connections. In the words of the Appellants:

> Electronic systems and devices are being required to perform more functions in shorter periods of time. Such electronic systems and devices contain multiple semiconductor chips, circuits and or the like. The semiconductor chips or circuits are typically required to communicate with each other in order to perform particular operations or functions. To accomplish these communications, multiple communications links or conductors are required to interconnect the semiconductor chips or circuits. These electrical connections can occupy considerable area on a substrate and can also require multiple pins on each of the chips for the inter-chip communications. Complex software may also be needed to implement the inter-chip or circuit communications and to accurately direct or address data signals or information to various components to perform the particular functions or operations.
>
> Accordingly, for the reason stated above, and for other reasons that will become apparent upon reading and understanding the present specification, there is a need for a multiple channel communications interface that minimizes the number of inter-chip connects and pins on each chip. Additionally, there is a need for a multiple channel communications interface that simplifies the software required for implementation and minimizes overhead, and is scalable to provide more or fewer communications channels depending upon design constraints. (Specification, Page 1)

Claim 1 is exemplary:

1. A communications interface, comprising:

a bus interface coupleable to an internal bus;

a plurality of transmit channels coupled to the bus interface;

a transmit control block coupled to the plurality of transmit channels;

a plurality of outbound links coupled to a plurality of outputs of the transmit control block;

a plurality of receive channels coupled to the bus interface; and

a receive control block coupled to the plurality of receive channels; and

a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface; and

a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Vernon	US 5,088,024	Feb. 11, 1992
Dahlen	US 5,317,749	May 31, 1994
Fung	US 5,396,635	May 07, 1995
Holm	US 6,122,680	Sept. 19, 2000
Earnest	US 6,226,338 B1	May 01, 2001 (filed Jun. 18, 1998)

Baker	US 6,333,938 B1	Dec. 25, 2001 (filed Apr. 29, 1997)
Bennett	US 6,697,904 B1	Feb. 24, 2004 (filed Mar. 28, 2000)
Gulick	US 6,816,935	Nov. 09, 2004 (filed Mar. 2, 2001)

Group I: Claims 1 to 14, 16 to 18, 28 to 31, 33 to 34, 36 to 44, and 49 stand rejected under 35 U.S.C. § 103(a) for being obvious over Baker in view of Earnest.

Group II: Claim 35 stands rejected under 35 U.S.C. § 103(a) for being obvious over Baker in view of Earnest in view of Holm.

As the issues described below apply to both groups of claims, they will be considered together.

Appellants contend that the claimed subject matter is not rendered obvious by Baker in combination with Earnest and Holm as the references were not properly combined, and the combination of references fails to disclose some of the claimed subject matter. These contentions will be discussed more fully below.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).[2]

[2] Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a

We affirm the rejections.

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether there is a legally sufficient justification for combining the disclosures of Baker and Earnest for all the claims, and Holm for claim 35. Additional issues address Appellants' contention that the references do not disclose claimed limitations of the invention.

FINDINGS OF FACT

Findings with respect to the rejection of claims 1 to 14, 16 to 18, 28 to 31, 33 to 44, and 49 under 35 U.S.C. § 103(a):

1. Appellants have invented a method and apparatus for transmitting data between semiconductor chips on an internal bus in a computer or related device, using multiple communication interfaces with a plurality of transmit and a plurality of receive channels coupled to bus interfaces to bear the burden of transmitting and receiving data between the chips. (Specification 1; claim 1). Stop and start message channels control the flow of data to a receiving First In First Out buffer device (FIFO), adapted to send a stop message to a source when the FIFO reaches a stop threshold value, and send a start message to the source when a start threshold value in the FIFO is reached. (Specification 17 middle; claim 1)

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separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young,* 927 F.2d 588, 590, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii).

2. Baker teaches an interface device compatible with computer industry standards for controlling the transfer of data packets between devices in a computer environment. (Col. 5, l. 24). Reading Baker's PCI-Serial Bus Interface #20 (Figure 1) as the claimed interface device, including from Figure 2 DMA Logic 72 and LLC Logic 90, we read the elements of claim 1 on Baker as expressed by the Examiner on page 3 of the Answer.

3. The operation of this device is explained by Baker in column 19, lines 7 to 16.

> While moving data from GRF 80 [General Receive FIFO] to the PCI interface logic 70, DMA engine 74 waits for GRF 80 to have sufficient data before requesting the PCI bus master to perform a transfer. This transfer threshold is reached whenever one of two conditions is met. DMA engine 74 will request a transfer of the PCI master whenever the number of bits in the receive FIFO reaches a "high water mark". This high water mark is equal to the greater of the cache line size register or the lower bound field of the DMA global register.

4. It is noted that this operation holds, or stops, the transfer of data from the receive FIFO until the number of bits in the receive FIFO reaches a certain threshold, after which a signal commences the transfer from the FIFO.

5. Earnest teaches a multi-channel data interface controller in which single FIFO transmit and receive circuits communicate through a plurality of logical channels. (Earnest, Col. 2). To

control the flow of data, Earnest teaches using different flags on different output channels to indicate start and stop messages. (Earnest, Col. 11, ll. 35 to 45). We find that Earnest is working in the same field of endeavor, communication channels for DMA controllers with data interface controllers, as Baker. Indeed, they are addressing the same problem, namely managing communications between the DMA engines and the interface.

6. We observe in the record of transactions of this prosecution, as indicated in the PALM records and documents on file, that in the Final Rejection mailed November 5, 2004, the Examiner took Official Notice concerning the power savings circuits being common in the prior art. Appellants did mention the Official Notice in the Amendment after Final Rejection filed March 10, 2005, but we find that the Examiner's use of Official Notice was not traversed. Appellants instead mentioned that changes in the independent claim rendered the subject claim allowable. However, it is noted that the Examiner did nonetheless support his Official Notice of power circuits and the round-robin algorithm with the submissions of Fung, Gulick, Dahlen and Vernon, used solely to bolster his statement of Official Notice. (Examiner's Answer 12).

7. Appellants contend that Claims 4 and 5 recite long lists of different registers, not clearly pointed out by the Examiner to be in the Baker reference. (Br. 15). We find that the wordings of

these claims include the language "wherein the plurality of transmit (receive) control registers comprises at least one of". (Emphasis added). Considering this limitation's wording, we find the claim language met as indicated in the rejection by the recitation of just a few of the registers. We find a similar argument with respect to claim 16 similarly met by Examiner's pointing out the direct control mode in Baker.

8. With respect to Claim 30, we find that the claimed limitation of selecting alternative transmit and receive FIFOs when a first one is not available is taught by Baker, for reasons cited by Examiner. (Answer 13, middle).

9. With respect to Claim 35, Examiner contends that Holm teaches a data bus width "can be any size and the clock rate can be any speed" (Holm, col. 8, l. 32) and the claimed limitation of a nibble, two-bit or serial width would be a design choice within the abilities of the practitioner in this art. We find no evidence of an error in this statement.

PRINCIPLES OF LAW

On appeal, Appellants bear the burden of showing that the Examiner has not established a legally sufficient basis for the rejection of the claims.

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

We note our reviewing court has recently reaffirmed that:

> an implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the 'improvement' is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient ... In such situations, the proper question is whether the ordinary artisan possesses knowledge and skills rendering him *capable* of combining the prior art references.

DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co., 464 F.3d 1356, 1368, 80 USPQ2d 1641, 1651 (Fed. Cir. 2006) (emphasis in original).

References within the statutory terms of 35 U.S.C. § 103 qualify as prior art for an obviousness determination only when analogous to the claimed invention. *In re Clay*, 966 F.2d 656, 658, 23 USPQ2d 1058, 1060 (Fed. Cir. 1992). Two separate tests define the scope of analogous prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed and, (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved. *In re Deminski*, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986); see also *In re Wood*, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979) and *In re Bigio*, 381 F.3d 1320, 1325, 72 USPQ2d 1209, 1212 (Fed. Cir. 2004). Furthermore, "'there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness' . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would

employ." *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)).

ANALYSIS

Appellants contended that Examiner erred in rejecting claims 1 to 14, 16 to 18, 28 to 31, 33 to 44, and 49 under 35 U.S.C. § 103(a). Reviewing the findings of facts cited above, we observe the claimed subject matter to be found in the Baker reference, especially in view of Earnest and, with respect to claim 35, the Holm reference.

Appellants have argued that the proper steps to establish a motivation to combine the references has not been presented by the Examiner. (Brief, page 12). We perceive that the analysis used by the Examiner is consistent with the lessons of our guiding court in *Kahn* and *Dystar*, which was endorsed by the Supreme Court in the recent *KSR* opinion (cases cited above). The Baker reference teaches the main claimed invention of the Appellants, but Earnest and Holm, in addressing a problem similar to that of Baker and that of the Appellants (transferring data from FIFO registers in a computer interface) demonstrated the prior art to teach other aspects of the claimed invention. Examiner has particularly pointed out which limitations were shown and not shown in Baker (Answer, 3 and 4). Examiner has then shown where those teachings are to be found elsewhere in the prior art, in the same field of endeavor and, in this case, addressing the same problem. *KSR* teaches that the secondary reference need not be solely addressing the Appellants' problem. "The second error of the Court of Appeals lay in its assumption that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same

problem." (*KSR Int'l v. Teleflex Inc.*, 127 S. Ct. at 1742, 82 USPQ2d at 1397 (2007). Examiner demonstrated that the claimed limitations are within the prior art, in references within the same field of endeavor, and addressing the Appellants' problem on the way to addressing their own.

Concerning the procedural issue of citing references to establish the Examiner's Official Notice of a known technology, we see no error for this tribunal to address.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have not established that claims 1 to 14, 16 to 18, 28 to 31, 33 to 44, and 49 were rejected in error. We will affirm the rejections.

DECISION

The Examiner's rejection of claims 1 to 14, 16 to 18, 28 to 31, 33 to 44, and 49 is Affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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